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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,573	04/26/2001	Michael J. Demler	ANTR-01020us1	1067
23910	7590	09/07/2005	EXAMINER	
FLIESLER MEYER, LLP FOUR EMBARCADERO CENTER SUITE 400 SAN FRANCISCO, CA 94111			STEVENS, THOMAS H	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/843,573

Applicant(s)

DEMLER ET AL.

Examiner

Thomas H. Stevens

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/14/05 & 6/17/05.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 June 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

RS

DETAILED ACTION

1. Claims 1-24 were examined.

Section I: Final Rejection (2nd Office Action)

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) is required in this application because most of the hand written annotations (e.g., figure 4) is unclear. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. **Claims 1-15, 19-23** are rejected under 35 U.S.C. 103(a) as being obvious over Killian et al (U.S. Patent Number 6,477,683), herein referred to as **Killian** and further in view of **Mendel** and in further view of **Havens** (U.S. Patent 6,345,240 (2002)).
4. As to **Claims 1 and 10**, **Killian** teaches: a method of optimizing performance characteristics in circuit synthesis, comprising the steps of: (a) generating a set of circuit parameters for each performance characteristic of a circuit (**column 17, lines 30-32**); (b) passing circuit parameters through a respective circuit model (**column 17, lines 32-36 and column 23, line 47, "HDL model"**), wherein additional sets of circuit parameters may be passed at the same in parallel (**Claims 1 and 10, Havens: column 2, lines 23-24 with figure 3**); and (c) running a simulation of said circuit model on an analysis test bench in order to measure performance of said circuit model using said set of circuit parameters, the analysis test bench adapted to model circuitry external to said

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circuit and control the type of analysis to be performed for each said performance characteristic of said circuit (**column 23 line 46-column 24, line 3**); receiving the performance measurements for each simulation at an optimizer and determining for which performance characteristics the specifications are met, and, for those analyses where the specifications are not met then generating new parameter values and repeating steps (a) through (d) (**Heavens: abstract**).

5. **Killian** does not expressly teach the simultaneous passing of circuit parameters and multiple test benches nor parallel simulation.

6. **Mendel** teaches a parallel processing system that includes the simultaneous passing of circuit parameters and multiple test benches (**Figure 3A**) wherein compilation includes simulation (**column 6, lines 27-32**) since parallel processing uses multiple CPUs to work on different aspects of the compilation project simultaneously, thus reducing the total amount of time it takes to compile the entire project (**column 14, lines 48-51**) which is important since longer development times greatly slow the time to market and slow development can erase any commercial advantage (**column 3, lines 6-12**).

Heavens teaches a simulation task generator that receives a range of parameters that are desired for a particular parallel simulation.

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the optimizing steps as taught in **Killian** to include the functionality for a parallel processing system allowing the simultaneous passing of circuit parameters and multiple test benches as taught in **Mendel** since parallel

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processing uses multiple CPUs to work on different aspects of the compilation project simultaneously, thus reducing the total amount of time it takes to compile the entire project (**column 14, lines 48-51**) which is important since longer development times greatly slow the time to market and slow development can erase any commercial advantage (**column 3, lines 6-12**) as taught in **Mendel**. Furthermore, the invention provides for a simulation task generator that reduces the effort and time required for a user to prepare for a parallel simulation (**column 1, lines 38-40**) as taught in **Heavens**.

8. As to **Claims 2 and 11**, **Killian** teaches: the step of receiving the measurements of performance for each simulation in an optimizer, said optimizer adapted to determine whether specifications were met for said simulation (**column 6, lines 62-64 and column 18, lines 47-64**).

9. As to **Claim 3, 4 and 13**, **Killian** teaches: the step of generating new set of circuit parameter values in said optimizer (**column 18, lines 61-67**); passing said new set of circuit parameter values through the respective said circuit model (**column 6, lines 62-64 and column 18, lines 61-67**) wherein individual parameters of the design are changed and the circuit is iteratively optimized which would involve the changing and passing of new circuit parameters through the circuit model for further testing and optimizing.

10. As to **Claim 5**, **Mendel** teaches: assigning each said analysis to a separate processor for parallel processing (**Figure 3A and column 16, lines 14-18**).

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11. As to **Claim 6, Killian** teaches: the step of checking a lookup database for previously optimized performance characteristics (**column 18, lines 26-34 and column 19, lines 33-35**).

12. As to **Claim 7, Killian** teaches: the step of saving optimized performance characteristics to a lookup database (**column 19, lines 33-35**).

13. As to **Claim 8, Killian** teaches: the step of setting up ranges for each said analysis test bench and providing design parameters using a simulation script (**column 23, lines 46-58**) wherein the test programs include ranges for the test bench to determine if the circuit design is operating within the circuit specifications of the design.

14. As to **Claim 9, Killian** teaches: the step of mapping the function of a design parameter to a performance characteristic (**column 18, lines 20-23**) wherein the design parameters specified by the user constitutes goals for the performance characteristics of the design.

15. As to **Claim 12, Killian** teaches: said optimizer comprises an optimization algorithm (**column 18, lines 47-48, 59-61**).

16. As to **Claim 14, Mendel** teaches: a simulator for each said analysis test bench (**Figures 3A and 3B and descriptions**) wherein the compiler functions include simulating the design (**column 6, lines 28-33**).

17. As to **Claims 15, Mendel** teaches: each said analysis test bench is adapted to run multiple occurrences of said analysis for each said circuit (**Figure 3B and description**).

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18. As to **Claim 19, Mendel** teaches: a processor for each said circuit model **(column 17, lines 47-53)**.

19. As to **Claim 20, Mendel** teaches least one-simulation script for each said circuit model **(column 16, lines 2-15)**.

20. As to **Claim 21, Killian** teaches: a synthesis plan adapted to set out rules for said analysis **(column 7, lines 38-42)**.

21. As to **Claims 22 and 23, Killian** teaches: a lookup database wherein said lookup database includes a set of performance specifications for each said circuit model **(column 18, lines 26-34, 47-48 and column 19, lines 33-35)** wherein the input goals are performance specifications.

22. **Claims 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Killian and Mendel** as applied to **Claim 10** above, and further in view of Rajsuman et al (U.S. Patent Number 6,678,645), herein referred to as **Rajsuman**.

23. As to **Claims 16 and 17, Killian and Mendel** teach a simulation system (**Killian: column 23 line 46-column 24, line 3, Mendel: Figure 3B and description**).

24. **Killian and Mendel** does not expressly teach these settings including operating conditions such as temperature, supply voltage and fabrication process.

25. **Rajsuman** teaches various basic types of verification tests corresponding to different levels of design abstraction which include corner testing which is testing for complex scenarios and corner cases such as minimum and maximum conditions in voltage, temperature and process **(column 2, lines 16-25 and 28-30)**.

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26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to simulate the models as disclosed in **Mendel** over operating conditions such as temperature, supply voltage and fabrication process as taught in **Rajsuman** if the design in **Mendel** was a system on a chip IC that required basic verification tests such as corner testing as taught in **Rajsuman**.

27. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Killian and Mendel** as applied to Claim 10 above, and further in view of MicroSim ("MicroSim Pspice A/D & Basics+ Circuit Analysis Software, User's Guide", Version 8.0, June 1997, pages 1-2-1-14, 2-2-2-5), herein referred to as **MicroSim**.

28. As to **Claim 18**, **Killian and Mendel** teach a simulation system (**Killian: column 23 line 46-column 24, line 3, Mendel: Figure 3B and description**).

29. **Killian and Mendel** does not expressly teach circuitry is selected from the group consisting of stimuli, power supplies, and load devices.

30. **MicroSim** teaches software to simulate a design in which load devices and power supplies can be selected (**page 2-2, "To Place Voltage Sources", page 2-3, "To Place Other Components" such as resistors and capacitors**) and stimuli can be applied to the circuit being tested (**page 1-14, "Stimulus File"**). The software models the behavior of a circuit containing any mix of analog and digital device that can be used to test and refine a design before realizing the design in hardware (**page 1-2, first paragraph**).

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a simulation program as taught in **MicroSim** as the

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simulation system as taught in **Killian and Mendel** since **MicroSim** teaches software in which circuitry such as stimuli, power supplies and load devices can be chosen that can be used to test and refine a design before realizing the design in hardware (**page 1-2, first paragraph**).

32. **Claim 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Killian and Mendel** as applied to **Claim 10** above and further in view of Kang et al (Kang et al, "CMOS Digital Integrated Circuits, Analysis and Design", second Edition, WCB/McGraw Hill, 1999, chapter 4), herein referred to as **Kang**.

33. As to **Claim 24**, **Killian and Mendel** teach a simulation system (**Killian: column 23 line 46-column 24, line 3, Mendel: Figure 3B and description**).

34. **Killian and Mendel** do not expressly teach said design parameters are selected from the group consisting of transistor dimensions, bias current values, and adjustable circuit parameters.

35. **Kang** teaches a transistor model simulated in SPICE in which design parameters include the transistor dimensions (**page 118, last paragraph, L and W**), bias current values (**page 119, equation 119, where κ , γ , W and L can be specified and are used to calculate the current**) and adjustable circuit parameters (**page 122, paragraph above equation 4.5**) wherein these parameters can be specified.

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made that a common transistor model such as the one used for SPICE simulations could be used to simulate the design in **Killian and Mendel** if the design in **Killian and Mendel** required a transistor model analysis. Furthermore, in using this

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transistor model as taught in **Kang**, design parameters would be selected from the group consisting of transistor dimensions, bias current values, and adjustable circuit parameters (**page 118, last paragraph, L and W, page 119, equation 119, where κ , γ , W and L can be specified and are used to calculate the current, and page 122, paragraph above equation 4.5).**

Section II: Response to Applicants' Arguments

Amendment to the Specification Accepted

37. Applicants are thanked for addressing this issue. The Office acknowledges and accepts amended specification.

Nonstatutory Double Patenting

38. Applicants are thanked for addressing this issue. The office acknowledges and accepts Terminal Disclaimer for copending application 09/560,844; rejection is withdrawn.

Specification

39. Applicants are thanked for addressing this issue. Objection is withdrawn.

35 USC § 103

40. Applicants are thanked for addressing this issue. Rejection is withdrawn; however a new rejection is activated from applicants' amendment.

Conclusion

41. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Leo Picard at (571) 272-3749. Central Fax number is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

August 29, 2005


Paul L. Rodriguez 9/1/05
Primary Examiner
Art Unit 2125

THS